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About This Manual

This manual describes the operation of the TMS320C6201 ('C6201) test and evaluation board (TEB). The 'C6201 TEB is a low-cost desktop card that helps you evaluate certain characteristics of the 'C6201 digital signal processor (DSP) to determine if the DSP meets your application requirements. You can create your software to run on board and expand the system using the prototype area.

This manual tells you how to install and operate release 1.00 of the 'C6201 TEB with your system. It also does the following:

- Describes key features of the TEB
- Tells you how to install and operate the TEB
- Helps you understand the TEB’s key components

How to Use This Manual

This book is divided into three sections:

- **Introductory information**, consisting of Chapters 1 and 2. Chapter 1 provides an overview of the 'C6201 TEB, its components, and the organization of this book. Chapter 2 discusses the theory of hardware operation of the TEB.

- **Topical material**, consisting of Chapter 3, provides descriptions of hardware functions.

- **Reference material**, consisting of Appendixes A and B, provides PAL® code and schematics.
Notational Conventions

This document uses the following conventions.

- Program listings, program examples, and interactive displays are shown in a special typeface.
- Device names are abbreviated with a C, followed by the last two to four alphanumeric characters in the name. For example, TMS320C6x is written as ‘C6x and TMS320C6201 is written as ‘C6201.

Information About Cautions

This book contains cautions.

This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software or equipment.

The information in a caution is provided for your protection. Please read each caution carefully.
Related Documentation

You can use the following books to supplement this user’s guide:

*Programming Atmel’s AT29 Flash Family, Flash Application Note (AN-3)*
(Amtel literature number 0518B)

Related Documentation From Texas Instruments

The following books describe the 'C6x devices and related support tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924. When ordering, please identify the book by its title and literature number.

*XDS51x Emulator Installation Guide* (literature number SPNU070) describes the installation of the XDS510™, XDS510PP™, and XDS510WS™ emulator controllers. The installation of the XDS511™ emulator is also described.

*JTAG/MPSD Emulation Technical Reference* (literature number SPDU079) provides the design requirements of the XDS510™ emulator controller, discusses JTAG designs (based on the IEEE 1149.1 standard), and modular port scan device (MPSD) designs.

*TMS320C6x C Source Debugger User’s Guide* (literature number SPRU188) tells you how to invoke the 'C6x simulator and emulator versions of the C source debugger interface. This book discusses various aspects of the debugger, including command entry, code execution, data management, breakpoints, profiling, and analysis.

*TMS320C62xx Technical Brief* (literature number SPRU197) gives an introduction to the 'C62xx digital signal processor, development tools, and third-party support.

*TMX320C6201 Digital Signal Processor data sheet*, (literature number SPRS051).

*TMS320C62xx Peripherals Reference Guide* (literature number SPRU190) describes common peripherals available on the TMS320C62xx digital signal processors. This book includes information on the internal data and program memories, the external memory interface (EMIF), the host port, serial ports, direct memory access (DMA), clocking and phase-locked loop (PLL), and the power-down modes.

*TMS320C62xx CPU and Instruction Set Reference Guide* (literature number SPRU189) describes the 'C62xx CPU architecture, instruction set, pipeline, and interrupts for the TMS320C62xx digital signal processors.
TMS320C6x Software Tools Getting Started Guide (literature number SPRU185) describes how to install the TMS320C6x assembly language tools, the C compiler, the simulator, and the C source debugger. Installation instructions for SunOS™, Solaris™, Windows™ 95, and Windows NT™ systems are given.

TMS320C62xx Programmer’s Guide (literature number SPRU198) describes ways to optimize C and assembly code and includes application program examples.

TMS320C6x Optimizing C Compiler User’s Guide (literature number SPRU187) describes the ‘C6x C compiler. This C compiler accepts ANSI standard C source code and produces assembly language source code for the ‘C6x generation of devices. This book also describes the assembly optimizer, which helps you optimize your assembly code.

TMS320C6x Assembly Language Tools User’s Guide (literature number SPRU186) describes the assembly language tools (assembler, linker, and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the ‘C6x generation of devices.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.
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  - TI Online: http://www.ti.com
  - DSP Solutions: http://www.ti.com/dsps
  - 320 Hotline On-line: http://www.ti.com/sc/docs/dsps/support.htm

- North America, South America, Central America
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  - TI Literature Response Center U.S.A.: (800) 477-8924
  - Software Registration/Upgrades: (214) 638-0333 Fax: (214) 638-7742
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  - DSP Hotline: (281) 274-2320 Fax: (281) 274-2324 Email: dsph@ti.com
  - DSP Modern BBS: (281) 274-2323
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    - Email: comments@books.sc.ti.com

- Note: When calling a Literature Response Center to order documentation, please specify the literature number of the book.
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2 Installing the TMS320C6201 Test and Evaluation Board ...................... 2-1
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3–5 Shunt Jumpers ................................................................. 3-8
3–6 DIP Switches ................................................................. 3-10
The TMS320C6201 test and evaluation board (TEB) helps you evaluate certain characteristics of the TMS320C6201 (‘C6201) fixed-point digital signal processor (DSP) to ensure that it meets your application requirements. The TEB is a self-contained device, requiring connections to an ac power supply and to your own emulation hardware and software. The TEB is platform independent and uses either an XDS510™ for a PC™ or an XDS510WS™ emulator for a UNIX™ workstation.

The ‘C6201 TEB carries a ‘C6201 DSP on board to allow full-speed verification of ‘C6201 code. You can also use the TEB to design your own prototype systems. The ‘C6201 DSP has 1Mb on-chip SRAM that consists of 512Kb internal program/cache and 512Kb internal data memory. The TEB uses the ‘C6201’s 32-bit external memory interface to facilitate accesses to on-board synchronous and asynchronous memories. A PC or UNIX windows-oriented debugger simplifies code development and debugging. For more information about the debugger, refer to the TMS320C6201 C Source Debugger User’s Guide or TMS320C6x C Source Debugger User’s Guide for SparcStation.

The TEB also has a ‘C6201 16-bit host access port, an IEEE Std. 1149.1-compliant JTAG connector for accessing the ‘C6201’s scan-based emulation features, and a through-hole area for design prototyping. You can also use the TEB as a reference when designing your own systems.

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1.1 Key Features of the TMS320C6201 TEB | 1-2  
1.2 Functional Overview of the TMS320C6201 TEB | 1-3
1.1 Key Features of the TMS320C6201 TEB

The 'C6201 TEB has the following features:

- 'C6201 capable of executing 1600 million instructions per second (MIPS)
- Varied instruction cycle time:
  - 5-ns instruction cycle time when using the DSP's internal memories and the PLL in multiply-by-one mode
  - 7.5-ns instruction cycle time when using the TEB's external SBSRAM, regardless of which other TEB memories are used
- 128KB 7.5-ns synchronous burst static RAM (SBSRAM)
- 256KB 12-ns asynchronous static RAM (ASRAM)
- 128KB 200-ns Flash programmable erasable ROM (PEROM)
- 16-bit host port connector
- Emulator connector
- Prototyping area
1.2 Functional Overview of the TMS320C6201 TEB

Figure 1–1 shows the basic block diagram and interconnects of the 'C6201 TEB. The interconnects include the external memory, host port, and emulation interfaces.

The 'C6201 DSP interfaces to the memories through a 32-bit data bus. Headers are situated between the synchronous and asynchronous memories to allow easy examination of the external memory interfaces, address, data, and control signals. The TEB’s control signals are also available at these headers. Additional headers between the asynchronous memories and the prototyping area allow for access to asynchronous control signals and the data bus, which may be used in the prototyping area.

Use the host port connector to connect your host processor to the 'C6201’s host port interface. This allows your host processor to access the 'C6201’s internal data memory and also provides an alternative to the TEB’s DIP switches that are used for manual configuration of the EMIF.

An emulation connector provides access to the IEEE Std. 1149.1 (JTAG) scan-based emulation port of the 'C6201. This port is a superset of the IEEE 1149.1 standard and is used by either an XDS510 or XDS510WS emulator.
Figure 1–1. TMS320C6201 TEB Connectivity

- JTAG emulator connector
- Host port interface connector
- EMIF configuration DIP switches
- 'C6201 Emulation port
  - Host port data HD[15:0]
  - Host port address HA/DC[16:1]
- Buffering and observation headers
- SBSRAM 128KB
- ASRAM 256KB
- PEROM 128KB
- Buffering and prototype area headers
This chapter gives installation instructions for the 'C6201 TEB.

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<td>2-2</td>
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<td>2.2 Host Requirements</td>
<td>2-4</td>
</tr>
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<td>2.3 TMS320C6201 TEB Kit Components</td>
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<tr>
<td>2.4 TMS320C6201 TEB Connection</td>
<td>2-4</td>
</tr>
<tr>
<td>2.5 TMS320C6201 TEB Installation</td>
<td>2-7</td>
</tr>
</tbody>
</table>
2.1 The TMS320C6201 TEB

The 'C6201 TEB is 5 in x 12 in and is intended for desktop use. It meets the following specifications:

- Instruction cycles of 7.5-ns (frequency equal to 133 MHz). This is accomplished using a 33.25-MHz oscillator and operating the 'C6201’s phase-locked loop (PLL) in multiply-by-four mode.

- Configuration of the 'C6201’s external memory interface using the TEB’s on-board DIP switches. These switches are set for the following:
  - Use of the ‘C6201’s memory map 1
  - 128K byte SBSRAM in CE0 external address space (0x400000)
  - 128K byte PEROM in CE1 external address space (0x1400000) to be accessed in word-sized blocks
  - 256K byte ASRAM in CE2 external address space (0x2000000)
  - Boot-load startup of 16K words (64K byte) from the PEROM in CE1 external address space

- Use of the emulator’s TCLK signal

Figure 2–1 shows the layout of the ‘C6201 TEB.
Figure 2–1. TMS320C6201 TEB

- Emulation connector J2
- Oscillator U3
- Power connector J10
- Host port connector J4
- Reset S5
- Dip switches S2-S4
- Shunt jumpers JP3
- Dip switches S2-S4
2.2 Host Requirements

The TEB is platform independent and can be used with an XDS510 for a PC or XDS510WS emulator for a UNIX workstation. Refer to the TMS320C6x Emulator Installation Guide if you plan to use the TEB with a PC. See TMS320C6x Workstation Emulator Installation Guide if you plan to use the TEB with a UNIX workstation. The XDS51x Emulator Installation Guide lists the minimum hardware and software requirements for your emulator.

2.3 TMS320C6201 TEB Kit Components

- C6201 TEB
- Custom power supply
- TMS320C6201 Test and Evaluation Board Technical Reference
- Diskette containing TEB diagnostic source, object code, and a README file

2.4 TMS320C6201 TEB Connection

Before you apply power to the TEB or connect the TEB to your emulator, see Tables 2–1 and 2–2 to ensure that all shunt jumpers and DIP switches are set to their default positions. Tables 3–5 and 3–6 contain complete descriptions of all shunt jumpers and DIP switches used on the TEB. See these tables before you change any default settings.
Table 2–1. Default Shunt Jumper Settings

_A–B indicates HIGH (1), B–C indicates LOW (0)_

<table>
<thead>
<tr>
<th>Name</th>
<th>Position</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROM protect</td>
<td>JP1</td>
<td>1–2</td>
<td>Flash PEROM write disabled</td>
</tr>
<tr>
<td>TCLK select</td>
<td>JP2</td>
<td>2–3</td>
<td>Use XDS51x emulator’s TCLK signal</td>
</tr>
<tr>
<td>NMI</td>
<td>JP3.1</td>
<td>B–C</td>
<td>Nonmaskable interrupt inactive</td>
</tr>
<tr>
<td>INT4</td>
<td>JP3.2</td>
<td>B–C</td>
<td>Interrupts INT4—INT7 inactive</td>
</tr>
<tr>
<td>INT5</td>
<td>JP3.3</td>
<td>B–C</td>
<td></td>
</tr>
<tr>
<td>INT6</td>
<td>JP3.4</td>
<td>B–C</td>
<td></td>
</tr>
<tr>
<td>INT7</td>
<td>JP3.5</td>
<td>B–C</td>
<td></td>
</tr>
<tr>
<td>PLLFREQ1</td>
<td>JP3.6</td>
<td>B–C</td>
<td>120 MHz &lt; CLKOUT1 ≤ 180 MHz</td>
</tr>
<tr>
<td>PLLFREQ2</td>
<td>JP3.7</td>
<td>A–B</td>
<td></td>
</tr>
<tr>
<td>PLLFREQ3</td>
<td>JP3.8</td>
<td>B–C</td>
<td></td>
</tr>
<tr>
<td>CLKMODE0</td>
<td>JP3.9</td>
<td>A–B</td>
<td>PLL multiply-by-four mode</td>
</tr>
<tr>
<td>CLKMODE1</td>
<td>JP3.10</td>
<td>A–B</td>
<td></td>
</tr>
<tr>
<td>RSV0</td>
<td>JP3.11</td>
<td>A–B</td>
<td></td>
</tr>
<tr>
<td>RSV1</td>
<td>JP3.12</td>
<td>B–C</td>
<td></td>
</tr>
<tr>
<td>RSV2</td>
<td>JP3.13</td>
<td>A–B</td>
<td></td>
</tr>
<tr>
<td>CMPTB</td>
<td>JP3.14</td>
<td>A–B</td>
<td>Revision 1.x TMS320C6201 installed</td>
</tr>
<tr>
<td>EMU0</td>
<td>JP3.15</td>
<td>A–B</td>
<td></td>
</tr>
<tr>
<td>EMU1</td>
<td>JP3.16</td>
<td>A–B</td>
<td></td>
</tr>
<tr>
<td>LEENDIAN</td>
<td>JP3.17</td>
<td>A–B</td>
<td>Little-endian mode addressing</td>
</tr>
<tr>
<td>AXRDY</td>
<td>JP3.18</td>
<td>A–B</td>
<td>External controller ready (to avoid stalling)</td>
</tr>
<tr>
<td>HOLDZ</td>
<td>JP3.19</td>
<td>A–B</td>
<td>Connects ‘C6201 to the system</td>
</tr>
<tr>
<td>Unused</td>
<td>JP3.20</td>
<td>No Shunt</td>
<td></td>
</tr>
<tr>
<td>Unused</td>
<td>JP3.21</td>
<td>No Shunt</td>
<td></td>
</tr>
<tr>
<td>Unused</td>
<td>JP3.22</td>
<td>No Shunt</td>
<td></td>
</tr>
<tr>
<td>Unused</td>
<td>JP3.23</td>
<td>No Shunt</td>
<td></td>
</tr>
<tr>
<td>INV_CLKOUT2Z</td>
<td>JP3.24</td>
<td>B–C</td>
<td>Inverts CLKOUT2 to become SDRAM_CLK</td>
</tr>
</tbody>
</table>
### Table 2–2. Default DIP Switch Settings

<table>
<thead>
<tr>
<th>Name</th>
<th>Position</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SWCONF</td>
<td>S2.1</td>
<td>OFF</td>
<td>Configuration done via DIP switches</td>
</tr>
<tr>
<td>SMAP_BOOT</td>
<td>S2.2</td>
<td>OFF</td>
<td>Use memory map 1</td>
</tr>
<tr>
<td>SCE0_TYPE1</td>
<td>S3.1</td>
<td>ON</td>
<td>Assign SBSRAM to 'C6201’s CE0 space</td>
</tr>
<tr>
<td>SCE0_TYPE0</td>
<td>S3.2</td>
<td>OFF</td>
<td></td>
</tr>
<tr>
<td>SCE2_TYPE1</td>
<td>S3.3</td>
<td>ON</td>
<td>Assign ASRAM to 'C6201’s CE2 space</td>
</tr>
<tr>
<td>SCE2_TYPE0</td>
<td>S3.4</td>
<td>ON</td>
<td></td>
</tr>
<tr>
<td>SCE1_WIDTH1</td>
<td>S3.5</td>
<td>OFF</td>
<td>Identify memory in 'C6201’s CE1 space as one word wide</td>
</tr>
<tr>
<td>SCE_WIDTH0</td>
<td>S3.6</td>
<td>ON</td>
<td></td>
</tr>
<tr>
<td>SBOOT_CNT2</td>
<td>S4.1</td>
<td>OFF</td>
<td>Boot DMA transfer 16K words</td>
</tr>
<tr>
<td>SBOOT_CNT1</td>
<td>S4.2</td>
<td>OFF</td>
<td>(when using DMA0 boot-load startup)</td>
</tr>
<tr>
<td>SBOOT_CNT0</td>
<td>S4.3</td>
<td>ON</td>
<td></td>
</tr>
<tr>
<td>SBOOT_SRC2</td>
<td>S4.4</td>
<td>ON</td>
<td>Use DMA0 boot-load startup</td>
</tr>
<tr>
<td>SBOOT_SRC1</td>
<td>S4.5</td>
<td>ON</td>
<td></td>
</tr>
<tr>
<td>SBOOT_SRC0</td>
<td>S4.6</td>
<td>OFF</td>
<td></td>
</tr>
</tbody>
</table>
2.5 TMS320C6201 TEB Installation

The 'C6201 TEB is connected to a power supply and an emulator. The following steps show how to connect the TEB to both.

- To connect the TEB:
  - Power up the emulator, then the TEB.

- To disconnect the TEB:
  - Power down the TEB, then the emulator.

Never disconnect or reconnect any cables or other hardware devices while power is applied to the emulator or TEB. Doing so can cause damage to your TEB.
Step 1: Install your emulation hardware and software.

Step 2: Insert the female end of the ac line cord into the power supply.

Figure 2–2. Attaching ac cord into power supply
Step 3: Connect the power supply’s male 6-pin connector into J10 of the TEB.

Figure 2–3. Connecting power supply to TEB
Step 4: With moderate downward pressure, connect the 14-pin keyed connector from your emulator to J2 on the TEB.

Figure 2–4. Connecting the emulator to the TEB

Step 5: Plug the male end of the power supply’s ac line cord into an ac outlet. This applies power to the TEB. An LED on the power supply and one on the TEB indicates that power is applied.
This chapter describes the C6201 TEB, its key components and how they operate. It also provides additional information on the TEB’s various interfaces.

The C6201 TEB consists of the following:

- Custom power supply
- TMS320C6201 TEB
  - Memory control
  - Power
  - Reset generation
  - Clock generation
  - Interrupt generation
  - ’C6x external memory interface
  - ’C6x host port interface
  - Emulation interface
  - Prototyping area
  - Shunt jumpers and DIP switches
- 3.5” floppy diskette

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<td>3-7</td>
</tr>
</tbody>
</table>
3.1 Custom Power Supply

A custom power supply provides 2.5-, 3.3-, and 5.0-V\textsubscript{DC} regulated supply voltages to the TEB when connected to an ac wall outlet. An LED on top of the power supply illuminates when it has been properly connected to ac power. The LED blinks when the power supply is connected to a wall outlet where the dc outlet is not connected to the TEB. The TEB's power supply must be loaded to regulate the voltages measured at its dc outlet. Voltages at the dc outlet without the load of the TEB appear unstable.

Figure 3–1. Power Supply DC Connector

![Power Supply DC Connector Diagram]

3.2 Power Requirements

LED D3 (located next to the power jack on the TEB) illuminates when power is applied to the 6-pin dc power jack J10. See Figure 2–4 for details about applying power to the TEB. Table 3–1 lists the appropriate fuse current ratings to protect of TEB components:

Table 3–1. TEB Fuse Ratings

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Label</th>
<th>Schematic reference designation</th>
<th>Rating</th>
<th>Purpose of Supply Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5</td>
<td>( V_{CC2} )</td>
<td>F2</td>
<td>7.0 A</td>
<td>'C6201 internals</td>
</tr>
<tr>
<td>3.3</td>
<td>( V_{CC3} )</td>
<td>F1</td>
<td>4.0 A</td>
<td>'C6201 I/Os and TEB 3.3-V components</td>
</tr>
<tr>
<td>3.3</td>
<td>( P_{VCC3} )</td>
<td>F5</td>
<td>0.75 A</td>
<td>Prototype area 3.3-V components</td>
</tr>
<tr>
<td>3.3</td>
<td>( H_{VCC3} )</td>
<td>F6</td>
<td>0.25 A</td>
<td>Host port reference voltage</td>
</tr>
<tr>
<td>5.0</td>
<td>( V_{CC5} )</td>
<td>F3</td>
<td>1.0 A</td>
<td>TEB 5.0-V components</td>
</tr>
<tr>
<td>5.0</td>
<td>( P_{VCC5} )</td>
<td>F4</td>
<td>0.5 A</td>
<td>Prototype area 5.0-V components</td>
</tr>
</tbody>
</table>
Use only fuses with ratings given in Table 3–1 to avoid damage to the TEB.
Do not draw more current than allowed by the fuses. This can damage the power supply and the TEB.

3.3 Reset Generation

At power up, power down, and during burnout conditions, a supply voltage supervisory circuit forces the ‘C6201 DSP into a reset condition. Pressing the push-button switch S5 also forces a reset. In either case, the ‘C6201’s reset line is active (low) for a period of at least 200 ms.

3.4 Clock Generation

The ‘C6201 DSP is designed to operate at frequencies up to 200 MHz. Two options for generation of the clock signal CLKI are provided on the TEB. A 68-Ω resistor installed in location R3 selects oscillator U3. Removing R3 and installing it as R2 selects the SMA connector J1 as the source for the CLKI signal. These options, combined with the ‘C6201’s internal phase-locked loop (PLL), allow you to experiment with different clock frequencies. Use of the PLL in multiply-by-two or multiply-by-four modes for a CLKOUT1 frequency other than 133 MHz will require the replacement of components R6, C2, and C3. See TMS320C6201 Digital Signal Processor data sheet for more information.

The factory default configuration of the TEB uses a 33.25-MHz oscillator to provide input to the ‘C6201’s PLL, which is set to operate in multiply-by-four mode. R3 is installed to select U3 as the source for the ‘C6201’s PLL. Shunt jumpers JP3.10 (CLKMODE1) and JP3.9 (CLKMODE0) select the clock multiply-by-four mode. Shunt jumpers JP3.8 (PLLFREQ3) and JP3.6 (PLLFREQ1) select a CLKOUT1 frequency range of 120–180 MHz. The oscillator and the PLL provide a CLKOUT1 signal that has a period of approximately 7.5 ns, a frequency of 133 MHz, and a duty cycle of approximately 50%.

You may operate the ‘C6201 internally at frequencies up to 200 MHz by reconfiguring shunt jumpers JP3.10–JP3.6 and replacing the CLKI source. You must also replace oscillator U3 with a higher frequency 5.0-V oscillator. You may use SMA connector J1 by removing and installing the 68 Ω resistor R3 in the location of R2. When increasing frequencies up to 133 MHz, refer to
3.5 Interrupt Generation

Pressing the push-button switch S5 generates a manual reset of the ‘C6201. Shunt jumpers JP3.1 (NMI) and JP3.2 (INT4)–JP3.5 (INT7) pull the ‘C6201’s external interrupts up or down. The factory default shunt jumper settings must be pulled low because these interrupts are rising-edge sensitive.

Figure 2–1 shows the connections for the interrupts on the upper right of the prototype area, just right of U26. You must remove the appropriate interrupt shunt jumper(s) to control these interrupts with non-TEB circuitry (for example, prototype circuitry).

3.6 External Memories

The TEB provides three different types of memory for the user to configure. The TEB’s memory types, their speeds, and organizations are listed in Table 3–2:

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>Designation</th>
<th>Timing (ns)</th>
<th>Organization</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBSRAM</td>
<td>U10</td>
<td>7.5</td>
<td>32Kb x 32 bits</td>
<td>128 KB</td>
</tr>
<tr>
<td>ASRAM</td>
<td>U20–U21</td>
<td>12</td>
<td>64Kb x 16 bits</td>
<td>256 KB</td>
</tr>
<tr>
<td>ROM</td>
<td>U22–U25</td>
<td>200</td>
<td>32Kb x 8 bits</td>
<td>128 KB</td>
</tr>
</tbody>
</table>

**TEB Memory Configuration**

The ‘C6201 latches the levels of dual purpose signals HA/DC[13:1] at reset. These signals source the external bus control and the direct memory access (DMA) controller configuration registers in the ‘C6201. These signals and their use at reset are listed in Table 3–3 and Table 3–4:
Table 3–3. Sources for External Bus Control Registers at Reset

<table>
<thead>
<tr>
<th>Pin</th>
<th>Use of signal(s) at Reset</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>HA/DC[1]</td>
<td>MEM_MAP</td>
<td>Defines the memory map used for off-chip boot or internal RAM boot</td>
</tr>
<tr>
<td>HA/DC[3:2]</td>
<td>CE0_TYPE[1:0]</td>
<td>Defines the type of memory used in the CE0 external memory address space</td>
</tr>
<tr>
<td>HA/DC[5:4]</td>
<td>CE2_TYPE[1:0]</td>
<td>Defines the type of memory used in the CE2 external memory address space</td>
</tr>
<tr>
<td>HA/DC[7:6]</td>
<td>CE1_WIDTH[1:0]</td>
<td>Defines the width of asynchronous memories used in the CE1 memory address space</td>
</tr>
</tbody>
</table>

Table 3–4. Sources for DMA Controller Configuration Registers at Reset

<table>
<thead>
<tr>
<th>Pin</th>
<th>Use of signal(s) at Reset</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>HA/DC[10:8]</td>
<td>BOOT_CNT[2:0]</td>
<td>Defines the number of words to transfer</td>
</tr>
</tbody>
</table>

TEB ’C6201 EMIF and DMA Controller

The TEB offers two options for configuring the ’C6201’s EMIF and DMA controller at reset. DIP switch S2.1 selects the signals used in the multiplexer (U6 and U7 in Figure 2–1). When S2.1 is open, DIP switches S2.2, S3.1–6, and S4.1–6 configure the ’C6201. When S2.1 is closed, a host processor connected to host port connector J4 configures the ’C6201. Figure 3–2 shows configuration of the EMIF via the host port.

Figure 3–2. Configuration of the EMIF and DMA controller
The factory default setting of DIP switch S2.1 (SWCONF open) causes the remaining switches of S2—S4 to configure the TEB at reset. TEB memory logic, is contained in PAL® U8 and U9. Factory programmed PAL® equations (see Appendix A) latch the state of signals CE0_TYPE[1:0] and CE2_TYPE[1:0]. The latched value of these signals and the currently active chip enable CE0Z, CE1Z, or CE2Z from the ‘C6201, which are logically evaluated to determine which memory must be accessed. This means that only a single memory type controls the external memory bus at any given time. TEB memory logic signals the following changes: SBSRAM_CEZ enables the TEB’s SBSRAM, ASRAM_CEZ enables ASRAM, and ROM_CEZ ASRAM enables ROM.

3.7 Host Port Connection

Connector J4 connects to the TEB and an off-board (user supplied and programmed) host. You may select either a host connected to J4 or DIP switches to configure the external bus control and DMA Controller configuration registers at reset. See Figure 3–2 for more information.

This interface is verified to configure the EMIF and DMA controller but its performance with a host processor is not tested or guaranteed. The connector is a 2-row x 25-pin (0.50 in x 0.50 in) Samtec FTSH–125–01–L–DV–EJ.

3.8 Emulation Port Connection

Emulation connector J2 connects the ‘C6201’s emulation port and either the XDS510 or XDS510WS emulator. Shunt jumpers JP3.15 and JP3.16 pull the EMU0 and EMU1 signal up or down. The factory default configuration causes these signals to be pulled up. For more information about emulation signals, see the JTAG/MPSD Emulation Technical Reference.

SMA connector J3 allows the user to provide an alternate TCK signal. To use the alternate TCK signal, shunt jumper JP2 must be moved from its factory default position to connect pins 1 and 2.
3.9 Prototyping Area

Figure 2–1 shows the through-hole area for prototyping located at the left end of the TEB. This area includes two sockets for user-programmable 3.3-V\textsubscript{dc} 22V10 PAL\textsuperscript{®} devices (U26 and U27). Fused 3.3-V\textsubscript{dc} (P\textsubscript{VCC3}) and 5.0-V\textsubscript{dc} (P\textsubscript{VCC5}) supply connections are provided at both the top and bottom edges of the prototyping area. Fuses protect against attempts to draw more current than are allowed by the power supply’s design. Ground connections are provided at the extreme left end of the prototyping area.

Connectors J8 and J9 provide connectivity to the ‘C6201’s EMIF data, address, and control busses. These 32-bit connectors provide a direct connection with the modern test equipment cables. (The Amp part number is 2–767004–2 and the mating connector part number is 767003–9.) All 32 bits of data are available at J8. Only 19 bits of address are available at J9 because the TEB’s prototyping area shares the ‘C6201’s external address space CE1 with the on-board PEROM. Consequently, only asynchronous devices may be interfaced to J8 and J9. PAL\textsuperscript{®} U9 logic equations (in Appendix A) control buffers between the asynchronous memory portion of the TEB and the TEB’s prototyping area.

The ‘C6201’s external interrupts are available as test points NMI and INT4–INT7. See Section 3.5, Interrupt Generation, for details about the use of these test points.

\begin{center}
\textbf{CAUTION}

Use only fuses with ratings given in Table 3–1 to avoid damage to the TEB.

Do not draw more current than allowed by the fuses. This can damage the power supply and the TEB.
\end{center}

3.10 Shunt Jumpers and DIP Switches

The on-board ‘C6201 and TEB devices can be configured by changing the settings of shunt jumpers and DIP switches described in Tables 3–5 and 3–6.
# Table 3–5. Shunt Jumpers

<table>
<thead>
<tr>
<th>Name</th>
<th>Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROM protect</td>
<td>JP1</td>
<td>Write protects Flash PEROM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1-2  Writes disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2-3  Writes enabled</td>
</tr>
<tr>
<td>TCLK select</td>
<td>JP2</td>
<td>Selects JTAG clock</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1-2  SMA connector (J3)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2-3  Emulation connector (J2)</td>
</tr>
<tr>
<td>NMI</td>
<td>JP3.1</td>
<td>Nonmaskable interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A-B  Active</td>
</tr>
<tr>
<td></td>
<td></td>
<td>B-C  Inactive</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NONE Controlled by other logic (prototyping area)</td>
</tr>
<tr>
<td>INT4</td>
<td>JP3.2</td>
<td>External interrupts: edge-driven (rising edge)</td>
</tr>
<tr>
<td>INT5</td>
<td>JP3.3</td>
<td>A-B  Active</td>
</tr>
<tr>
<td>INT6</td>
<td>JP3.4</td>
<td>B-C  Inactive</td>
</tr>
<tr>
<td>INT7</td>
<td>JP3.5</td>
<td>NONE Controlled by other logic (prototyping area)</td>
</tr>
<tr>
<td>PLLFREQ1</td>
<td>JP3.6</td>
<td>Selects one of five frequency ranges for the 'C6201 CLKOUT1 signal</td>
</tr>
<tr>
<td>PLLFREQ2</td>
<td>JP3.7</td>
<td></td>
</tr>
<tr>
<td>PLLFREQ3</td>
<td>JP3.8</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>B-C  B-C  B-C  0-60 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>B-C  B-C  A-B  60-120 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>B-C  A-B  B-C  120-180 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>B-C  A-B  B-C  180-240 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A-B  B-C  B-C  240-300 MHz</td>
</tr>
<tr>
<td>CLKMODE0</td>
<td>JP3.9</td>
<td>Clock mode select. Selects the multiplication factor of the input clock fre-</td>
</tr>
<tr>
<td>CLKMODE1</td>
<td>JP3.10</td>
<td>quency. CLKOUT1 is 1x, 2x, or 4x CLKIN:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>B-C  B-C  PLL multiply-by-one mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>B-C  A-B  Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A-B  B-C  PLL multiply-by-two mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A-B  A-B  PLL multiply-by-four mode</td>
</tr>
<tr>
<td>RSV0</td>
<td>JP3.11</td>
<td>Reserved</td>
</tr>
<tr>
<td>RSV1</td>
<td>JP3.12</td>
<td></td>
</tr>
<tr>
<td>RSV2</td>
<td>JP3.13</td>
<td></td>
</tr>
<tr>
<td>CMPTB</td>
<td>JP3.14</td>
<td>Device compatibility mode for first silicon</td>
</tr>
<tr>
<td>EMU0</td>
<td>JP3.15</td>
<td>TI emulation support</td>
</tr>
<tr>
<td>EMU1</td>
<td>JP3.16</td>
<td></td>
</tr>
</tbody>
</table>
Table 3–5. Shunt Jumpers (Continued)

<table>
<thead>
<tr>
<th>Name</th>
<th>Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LENDIAN</td>
<td>JP3.17</td>
<td>Selects endianess of addressing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>B-C Big endian</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A-B Little endian</td>
</tr>
<tr>
<td>AXRDY</td>
<td>JP3.18</td>
<td>External controller ready</td>
</tr>
<tr>
<td>HOLDZ</td>
<td>JP3.19</td>
<td>Hold request from host (EMIF bus arbitration)</td>
</tr>
<tr>
<td>UNUSED</td>
<td>JP3.20</td>
<td>Unused</td>
</tr>
<tr>
<td>UNUSED</td>
<td>JP3.21</td>
<td>Unused</td>
</tr>
<tr>
<td>UNUSED</td>
<td>JP3.22</td>
<td>Unused</td>
</tr>
<tr>
<td>UNUSED</td>
<td>JP3.23</td>
<td>Unused</td>
</tr>
<tr>
<td>INV_CLKOUT2Z</td>
<td>JP3.24</td>
<td>Inverts CLKOUT2 to become SDRAM_CLK used for SDRAM timing:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>B-C Inverted</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A-B Noninverted</td>
</tr>
</tbody>
</table>

**Note:**
- A-B indicates HIGH (1)
- B-C indicates LOW (0)
### Table 3–6. DIP Switches

<table>
<thead>
<tr>
<th>Name</th>
<th>Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SWCONF</td>
<td>S2.1</td>
<td>Selects TEB method for EMIF configuration.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ON Host processor configures EMIF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF DIP switches configure EMIF</td>
</tr>
<tr>
<td>SMAP_BOOT</td>
<td>S2.2</td>
<td>Selects 'C6201 memory map.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ON Memory map 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF Memory map 1</td>
</tr>
<tr>
<td>SCE0_TYPE1</td>
<td>S3.1</td>
<td>Selects a memory type for external memory space CE0.</td>
</tr>
<tr>
<td>SCE0_TYPE0</td>
<td>S3.2</td>
<td>S3.1 S3.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ON ON Asynchronous memories (ASRAM, ROM)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ON OFF SBSRAM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF ON Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF OFF SDRAM</td>
</tr>
<tr>
<td>SCE2_TYPE1</td>
<td>S3.3</td>
<td>Selects a memory type for external memory space CE2.</td>
</tr>
<tr>
<td>SCE2_TYPE0</td>
<td>S3.4</td>
<td>S3.3 S3.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ON ON Asynchronous memories (ASRAM, ROM)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ON OFF SBSRAM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF ON Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF OFF SDRAM</td>
</tr>
<tr>
<td>SCE1_WIDTH1</td>
<td>S3.5</td>
<td>Selects the width of the asynchronous memories in the external memory space CE1</td>
</tr>
<tr>
<td>SCE1_WIDTH0</td>
<td>S3.6</td>
<td>S3.5 S3.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ON ON Byte</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ON OFF Halfword</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF ON Word</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF OFF Reserved</td>
</tr>
<tr>
<td>SBOOT_CNT2</td>
<td>S4.1</td>
<td>Selects the length of the boot DMA transfer.</td>
</tr>
<tr>
<td>SBOOT_CNT1</td>
<td>S4.2</td>
<td>S4.1 S4.2 S4.3</td>
</tr>
<tr>
<td>SBOOT_CNT0</td>
<td>S4.3</td>
<td>ON ON ON 256 words</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ON ON OFF 512 words</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ON OFF ON 1 024 words</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ON OFF OFF 2 048 words</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF ON ON 4 096 words</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF ON OFF 8 192 words</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF OFF ON 16 384 words</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF OFF OFF 32 768 words</td>
</tr>
<tr>
<td>SBOOT_SRC2</td>
<td>S4.4</td>
<td>Selects the startup mode after RESET.</td>
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<tr>
<td>SBOOT_SRC1</td>
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<td>S4.4 S4.5 S4.6</td>
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<tr>
<td>SBOOT_SRC0</td>
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<td>ON ON ON Direct execution startup</td>
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Appendix A

TMS320C6201 TEB PAL® Equations

This appendix contains the programmable logic source for the TMS320C6201 test and evaluation board PAL® equations. These were compiled with DATA I/O ABEL™ version 4.0.

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A.1 Memory Logic Block A

module U8_MLA
Title 'PAL NAME    Memory Logic Block A (PAL MLA)
PAL #       U8, D600555–1741*
DWG NAME    TMS320C6201 Test & Evaluation Board
ASSY #      D600550–0001A
COMPANY     Texas Instruments, Incorporated

SYNTHESIS TOOL: ABEL–4 Design Environment v1.0’

U8 device ‘P22V10C’; “The PALLV22V10 is a 28-pin PLCC
"NC         pin  1; NO CONNECT
clkout1     pin  2; "Clock out 1 from C6201
resetz      pin  3; "Reset
ce0_type0   pin  4; "Memory type in external memory space 0 – msb
ce0_type1   pin  5; "Memory type in external memory space 0 – lsb
ce2_type0   pin  6; "Memory type in external memory space 2 – msb
ce2_type1   pin  7; "Memory type in external memory space 2 – lsb
"NC         pin  8; NO CONNECT
ce0z        pin  9; "CE0 addr space enable
celz        pin 10; "CE1 addr space enable
ce2z        pin 11; "CE2 addr space enable
axwez       pin 12; "Asynchronous write enable
eal9        pin 13; "EMIF addr bit 19
GND         pin 14; "Ground
"NC         pin 15; NO CONNECT
illmla      pin 16; "Unused
ssram_cez   pin 17; "Synchronous Burst SRAM chip enable
sdram_cez   pin 18; "Synchronous DRAM chip enable
asram_cez   pin 19; "Asynchronous Static RAM chip enable
rom_cez     pin 20; "ROM chip enable
rce0_type1  pin 21 istype 'reg';
"NC         pin 22; NO CONNECT
ax_oez      pin 23; "Asynchronous output enable
ax_dir      pin 24; "Asynchronous direction
rce0_type0  pin 25 istype 'reg';
rce2_type1  pin 26 istype 'reg';
rce2_type0  pin 27 istype 'reg';
VCC         pin 28; "Power

Declarations "for brevity in equations and test vectors

Equations
clk = clkout1;
c = .c.;
rx = resetz;
c0t1 = ce0_type1;
c0t0 = ce0_type0;
c2t1 = ce2_type1;
c2t0 = ce2_type0;
rc0t1 = rce0_type1;
rc0t0 = rce0_type0;
rc2t1 = rce2_type1;
rc2t0 = rce2_type0;
asez = asram_cez;
ssez = ssram_cez;
sdez = sdram_cez;
rmez = rom_cez;

"Register the values of the chip enable type settings
"at reset OR the values fed back when not in reset.
rc0t1 := (!rz & c0t1) # (rz & rc0t1);
rc0t0 := (!rz & c0t0) # (rz & rc0t0);
rc2t1 := (!rz & c2t1) # (rz & rc2t1);
rc2t0 := (!rz & c2t0) # (rz & rc2t0);

"The TMS320C6201 only allows one chip enable space to be
"active at a time. Therefore, it is not necessary to have
"equations that check for this possibility. That is, no
"exclusive ORing is required.
!asez = (!ce0z & !rc0t1 & !rc0t0) # (!ce2z & !rc2t1 & !rc2t0); "ASRAM = 00
!ssez = (!ce0z & !rc0t1 & rc0t0) # (!ce2z & !rc2t1 & rc2t0); "SSRAM = 01
!sdez = (!ce0z & rc0t1 & rc0t0) # (!ce2z & rc2t1 & rc2t0); "SDRAM = 11
!rmez = !celz & !ea19;

!ax_oez = (!ce0z & !rc0t1 & !rc0t0) # !celz # (!ce2z & !rc2t1 & !rc2t0);
ax_dir = !axwez; "A->B (i.e., DSP to external memories) when 1,
        "B->A (i.e., external memories to DSP) when 0
Test Vectors

\((\text{clk}, \text{rz}, \text{c0t1}, \text{c0t0}, \text{c2t1}, \text{c2t0}) \rightarrow [\text{rc0t1}, \text{rc0t0}, \text{rc2t1}, \text{rc2t0}])\)

Test to ensure that the ASRAM type can be registered for either memory space CE0 or CE2

\([c, 0, 1, 1, 1, 1] \rightarrow [1, 1, 1, 1] ;<\text{ASRAM}\)

\([c, 0, 0, 0, 0, 0] \rightarrow [0, 0, 0, 0] ;\]

Test to ensure that the SSRAM type can be registered for either memory space CE0 or CE2

\([c, 0, 1, 0, 1, 0] \rightarrow [0, 1, 0, 1] ;<\text{SSRAM}\)

\([c, 1, 1, 0, 1, 0] \rightarrow [0, 1, 0, 1] ;\]

Test to ensure that the RSVD type can be registered for either memory space CE0 or CE2

\([c, 0, 0, 1, 0, 1] \rightarrow [0, 1, 0, 1] ;\]

\([c, 1, 0, 1, 0, 1] \rightarrow [1, 0, 1, 0] ;<\text{RSVD}\)

Test to ensure that the SDRAM type can be registered for either memory space CE0 or CE2

\([c, 0, 0, 0, 0, 0] \rightarrow [0, 0, 0, 0] ;\]

\([c, 0, 1, 1, 1, 1] \rightarrow [1, 1, 1, 1] ;<\text{SDRAM}\)

\([c, 1, 0, 0, 0, 0] \rightarrow [1, 1, 1, 1] ;\]
Test_Vectors
((clk, rz, ce0z, celz, ce2z, axwez, c0t1, c0t0, c2t1, c2t0, ea19) -> [asez, ssez, sdez, rmez, ax_oez, ax_dir])

"ASRAM enable tests

[c, 0, 1, 1, 1, 0, 0, 0, 0, 0] -> [1, 1, 1, 1, 0];
[c, 1, 0, 1, 1, 1, 1, 1, 0, 0] -> [0, 1, 1, 1, 0, 0];
[c, 1, 0, 1, 0, 1, 0, 1, 1, 1] -> [0, 1, 1, 1, 0, 1];
[c, 1, 0, 0, 0, 1, 1, 1, 1, 0] -> [0, 1, 1, 1, 0, 0, 0];
[c, 1, 1, 0, 0, 1, 0, 1, 1, 0] -> [0, 1, 1, 1, 0, 0, 0];
[c, 1, 1, 1, 0, 0, 1, 0, 1] -> [0, 1, 1, 1, 0, 0, 0];
[c, 1, 1, 1, 0, 0, 1, 1, 0] -> [0, 1, 1, 1, 0, 1];
[c, 1, 1, 1, 0, 0, 1, 0, 0] -> [0, 1, 1, 1, 0, 1];
[c, 1, 1, 1, 0, 0, 1, 1, 1] -> [0, 1, 1, 1, 0, 1];
[index]

"SSRAM enable tests

[c, 0, 1, 1, 1, 0, 0, 0, 0, 0] -> [1, 1, 1, 1, 0];
[c, 1, 0, 1, 1, 1, 0, 1, 0, 0] -> [1, 1, 1, 1, 0];
[c, 1, 0, 1, 1, 0, 1, 0, 0, 0] -> [1, 1, 1, 0, 0, 0];
[c, 1, 1, 1, 0, 1, 1, 0, 0, 0] -> [1, 1, 1, 0, 1];
[c, 1, 1, 0, 1, 1, 0, 0, 0, 0] -> [1, 1, 1, 0, 1];
[c, 1, 1, 1, 0, 1, 0, 0, 0, 0] -> [1, 1, 1, 0, 1];
[c, 1, 1, 1, 0, 1, 1, 0, 0, 0] -> [1, 1, 1, 0, 1];
[c, 1, 1, 1, 0, 1, 1, 0, 0, 0] -> [1, 1, 1, 0, 1];
[index]

"RSVD

[c, 0, 1, 1, 1, 0, 0, 0, 0, 0] -> [1, 1, 1, 1, 0];
[c, 1, 0, 1, 1, 1, 0, 1, 0, 0] -> [1, 1, 1, 1, 0];
[c, 1, 0, 1, 1, 0, 1, 0, 0, 0] -> [1, 1, 1, 0, 0, 0];
[c, 1, 1, 1, 0, 1, 1, 0, 0, 0] -> [1, 1, 1, 0, 1];
[c, 1, 1, 0, 1, 1, 0, 0, 0, 0] -> [1, 1, 1, 0, 1];
[c, 1, 1, 1, 0, 1, 0, 0, 0, 0] -> [1, 1, 1, 0, 1];
[index]

"ROM active when celz active and ea19 is low - prevent bus contention between ROM and prototype area

[c, 1, 1, 0, 1, 0, 1, 0, 1, 0] -> [1, 1, 1, 0, 0];
[c, 1, 1, 0, 1, 0, 0, 1, 0, 1] -> [1, 1, 1, 0, 1];
[c, 1, 1, 0, 1, 0, 1, 1, 0, 1] -> [1, 1, 1, 1, 0];
[c, 1, 1, 0, 1, 0, 1, 1, 0, 0] -> [1, 1, 1, 1, 1];
[index]

"ROM inactive when celz active and ea19 is high - prevent bus contention between ROM and prototype area

[c, 1, 1, 0, 1, 0, 1, 0, 1, 0] -> [1, 1, 1, 0, 0];
[c, 1, 1, 0, 1, 0, 0, 1, 0, 1] -> [1, 1, 1, 0, 1];
[c, 1, 1, 0, 1, 0, 1, 1, 0, 1] -> [1, 1, 1, 1, 0];
[c, 1, 1, 0, 1, 0, 1, 1, 0, 0] -> [1, 1, 1, 1, 1];
[index]

"SDRAM enable tests

[c, 0, 1, 1, 1, 0, 1, 0, 0, 0] -> [1, 1, 1, 1, 0];
[c, 1, 0, 1, 1, 1, 0, 0, 0, 0] -> [1, 1, 1, 1, 0];
[c, 1, 1, 0, 1, 1, 0, 0, 0, 0] -> [1, 1, 1, 1, 0];
[c, 1, 1, 0, 1, 1, 0, 0, 0, 0] -> [1, 1, 1, 1, 0];
[c, 1, 1, 0, 1, 1, 0, 0, 0, 0] -> [1, 1, 1, 1, 0];
[index]
end
A.2 Memory Logic Block B

module U9_MLB
Title
PAL NAME Memory Logic Block B (PAL MLB)
PAL # U9, D600555-1741*
DWG NAME TMS320C6201 Test & Evaluation Board
ASSY # D600550-0001A
COMPANY Texas Instruments, Incorporated

SYNTHESIS TOOL: ABEL-4 Design Environment v1.0'

U9 device 'P22V10C'; "The PALLV22V10 is a 28-pin PLCC

"NC" pin 1; NO CONNECT
b_clkout1 pin 2; "Buffered clock out 1 from C6201
resetz pin 3; "Reset
b_ce1z pin 4; "Buffered CE1 addr space enable
b_axwez pin 5; "Buffered asynchronous write enable
b_axoez pin 6; "Buffered asynchronous output enable
b_ea19 pin 7; "Buffered EMIF addr bit 19

"NC" pin 8; NO CONNECT
sswez pin 9; "SBSRAM write enable
sdwez pin 10; "SDRAM write enable
from_io7mla pin 11; "Feed forward from MLA
from_io8mla pin 12; "Feed forward from MLA
i10mlb pin 13; "Unused
GND pin 14; "Ground

"NC" pin 15; NO CONNECT
i11mlb pin 16; "Unused
p_cez pin 17; "Prototype area chip enable
p_oez pin 18; "Prototype area output enable
p_dir pin 19; "Prototype area direction
io3mlb pin 20; "Unused
io4mlb pin 21; "Unused

"NC" pin 22; NO CONNECT
io5mlb pin 23; "Unused
io6mlb pin 24; "Unused
io7mlb pin 25; "Unused
io8mlb pin 26; "Unused
io9mlb pin 27; "Unused
VCC pin 28; "Power

Equations
!p_cez = b_ea19 & !b_ce1z;
!p_oez = b_ea19 & !b_axoez;
p_dir = b_ea19 & !b_axwez;

Test_Vectors
(((b_ea19, b_ce1z) -> [p_cez])
[0, 0] -> [1];
[0, 1] -> [1];
[1, 0] -> [0];
[1, 1] -> [1];

Test_Vectors
(((b_ea19, b_axoez) -> [p_oez])
[0, 0] -> [1];
[0, 1] -> [1];
[1, 0] -> [0];
[1, 1] -> [1];

Test_Vectors
(((b_ea19, b_axwez) -> [p_dir])
[0, 0] -> [0];
[0, 1] -> [0];
[1, 0] -> [1];
[1, 1] -> [0];

end
This appendix contains the schematics for the TMS320C6201 TEB.
NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS.

2. CAPACITANCE VALUES ARE IN MICROFARADS.

3. HIGHEST REFERENCE DESIGNATOR USED:
   - A. CERAMIC CAPS C71
   - B. TANTALUM CAPS C79
   - C. DIODES D3
   - D. FUSES F6
   - E. CONNECTORS/HEADERS J11
   - F. SHUNT S73
   - G. FILTER L1
   - H. RESISTORS R114
   - I. SWITCHES S5
   - J. TEST POINTS TP127
   - K. IC'S U32

4. UNUSED REFERENCE DESIGNATORS:
   - A. DIODES D1
   - B. RESISTORS R4, R5, R80
   - C. SWITCHES S1
   - D. IC'S U2, U5

5. U1A-U1E COMPRISSE A SINGLE TMS320C6201. THIS IS A 352-CONTACT BGA DEVICE THAT IS TOO LARGE TO SHOW ON A SINGLE SHEET.

6. ALL FOUR SHIELD CONNECTIONS OF J1 AND J3 MUST CONNECT TO THE GROUND PLANE.

7. SHUNTS FOR M1 AND INT4-INT7, AS APPROPRIATE, MUST NOT BE PULLED UP (VCC) OR DOWN (GND) FOR CONTROL OF THESE SIGNALS IN THE PROTOTYPE AREA.

8. THE AXRDY SHUNT MUST NOT BE PULLED UP (VCC) OR DOWN (GND) FOR USE WITH AN EXTERNAL CONTROLLER.

REV

REV

REV

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