



# SmartModel Library Release Notes

To search the entire manual set, press this toolbar button.  
For help, refer to [intro.pdf](#).



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# Release Notes

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## Introduction

This document contains information about the following topics:

- [“What’s New?” on page 5](#)
- [“FlexModel Issues and Workarounds” on page 16](#)
- [“Getting Help” on page 17](#)

For general information about SmartModel Library documentation, or to navigate to a different online document, refer to the [Guide to SmartModel Documentation](#). For information about which platforms, operating systems, and simulators support SmartModels and FlexModels, refer to [SmartModel Library Supported Simulators and Platforms](#).

## What’s New?

These release notes are frequently updated to keep you informed about important changes in the SmartModel software or alert you to issues and workarounds that you should know about. You may find information about the following:

- [“Obsoleted Models, Unsupported Simulators and Platforms” on page 6](#)
- [“Models Ported to 64-bit Solaris and HPUX Systems” on page 6](#)

## Obsoleted Models, Unsupported Simulators and Platforms

Note the following major changes in Synopsys support for models, simulators, and workstation platforms:

- Synopsys has dropped support for all Microsoft Windows NT-based models.
- Synopsys has dropped support for Solaris 2.6.
- Synopsys has dropped support for HPUX 10.20.
- Synopsys has made obsolete its SmartCircuit family of simulation models. SmartCircuit models simulated FPGA devices. Current customers will have to use the free netlisting tools supplied by vendors rather than the FPGA SmartModels. Refer to the section “[FPGA SmartModel Obsolescence Notes](#)” on page 7 for additional information.
- The Cadence Verilog-XL simulator is no longer a supported simulator.
- Cadence’s NC-VHDL simulator does not support on any platform C-Flex based FlexModels when the control language is Vera. Cadence is aware of the problem and plans a future fix.

## Models Ported to 64-bit Solaris and HPUX Systems

Certain verification models have been ported so they will run with 64-bit simulators on 64-bit platforms. The only 64-bit platforms that Synopsys supports are HPUX 64-bit systems and Solaris 64-bit systems. You can determine if a particular model is available on a 64-bit version by using the search capabilities on the IP Directory web page. When you search and find a model, its summary page tells you whether the model is available in a 64-bit version

You can find the IP Directory at:

<http://www.synopsys.com/products/designware/ipdir/>

## FPGA SmartModel Obsolescence Notes

Effective December 1st 2003, the Synopsys FPGA SmartModel simulation models that are offered as part of the DesignWare Library will be obsolete. This section documents the transition and technical support plans.

This model obsolescence only affects the FPGA SmartModels and no other models are affected. A list of all the FPGA SmartModels can be found at the end of this document.

### Obsolescence Plan

Technical Support consists of the following:

- All Support for the FPGA SmartModels ends December 1, 2003.
- No model Enhancements will be implemented.
- Only critical B4 bugs will be fixed.

A B4 bug is defined as a problem that has no workaround and that causes work to stop at the site.

### Transitioning from FPGA SmartModels

Refer to [Table 1](#) to help you transition from the FPGA SmartModels. It lists SolvNet documents that explain how to use the FPGA vendor tools to simulate the post-routed FPGA netlist, replacing the FPGA SmartModels in your flow. These vendor-generated netlists offer full functional models with timing and are offered without cost

**Table 1: SolvNet Articles On Vendor FPGA Tools**

SolvNet Article Number	Title
004094	"How to simulate an Altera FPGA design netlist, in QuicksimII or Modelsim"
004177	"How to simulate a Xilinx FPGA design netlist, in Quicksim or Modelsim"
004958	"How to Simulate an Altera FPGA Design Netlist in Synopsys' VCS Simulator"
004960	"How to Simulate an Altera FPGA Design Netlist in MTI Modelsim-Verilog"
004961	"How to Simulate an Altera FPGA Design Netlist on Synopsys' Scirocco Simulator"

**Table 1: SolvNet Articles On Vendor FPGA Tools**

SolvNet Article Number	Title
004963	"How to Simulate an Altera FPGA Design Netlist on Cadence's NC-VHDL Simulator"
004964	"How to Simulate an Altera FPGA Design Netlist on Cadence's NC-Verilog Simulator"
004965	"How to Simulate a Xilinx FPGA Design Netlist in MTI Modelsim-Verilog"
004966	"How to Simulate a Xilinx FPGA Design Netlist on Cadence's NC-Verilog Simulator"
004969	"How to Simulate a Xilinx FPGA Design Netlist in Synopsys' VCS Simulator"
004968	"How to Simulate a Xilinx FPGA Design Netlist on Synopsys' Scirocco Simulator"
004967	"How to Simulate a Xilinx FPGA Design Netlist on Cadence's NC-VHDL Simulator"

**Altera:**

Quicksim or MTI-VHDL: <http://solvnet.synopsys.com/retrieve/004094.html>

MTI-Verilog: <http://solvnet.synopsys.com/retrieve/004960.html>

Scirocco: <http://solvnet.synopsys.com/retrieve/004961.html>

VCS: <http://solvnet.synopsys.com/retrieve/004958.html>

NC-Verilog: <http://solvnet.synopsys.com/retrieve/004964.html>

NC-VHDL: <http://solvnet.synopsys.com/retrieve/004963.html>

**Xilinx:**

Quicksim or MTI-VHDL: <http://solvnet.synopsys.com/retrieve/004177.html>

MTI-Verilog: <http://solvnet.synopsys.com/retrieve/004965.html>

Scirocco: <http://solvnet.synopsys.com/retrieve/004968.html>

VCS: <http://solvnet.synopsys.com/retrieve/004969.html>

NC-Verilog: <http://solvnet.synopsys.com/retrieve/004966.html>

NC-VHDL: <http://solvnet.synopsys.com/retrieve/004967.html>

If you have any further questions please feel free to contact Synopsys via the following email address:

<mailto:designware@synopsys.com>

Subject Line: FPGA SmartModel Obsolescence Query

## Obsolescence FAQ

*Are you obsolescing all the models?*

No, just the FPGA SmartModels. FPGA SmartModels are the programmable models of devices from Xilinx, Altera, Lattice and other vendors. The list follows this FAQ.

*What does the FPGA SmartModel obsolescence mean to me?*

If you are using the FPGA SmartModels you will have to transition to using the free netlisting tools supplied by the vendors rather than the FPGA SmartModels.

*How do the two models differ?*

Both FPGA SmartModels and the vendor-generated netlists offer full functional models with timing.

*Where can I find information on how to use the vendor tools to create the netlists?*

A list of transition documents are linked to above.

*Why is Synopsys obsolescing the FPGA SmartModels?*

Only a handful of Synopsys customers still use these models. Synopsys can better serve our customers by focusing our resources on Verification IP that can be used by a broad subset of our customers.

*What about Technical Support?*

All support end December 1st 2003

## List of Obsoleted FPGA SmartModels

a1010\_100 a1010\_44 a1010\_68 a1010\_84 a1020\_100 a1020\_44 a1020\_68 a1020\_84  
a1225\_100 a1225\_84 a1240\_132 a1240\_144 a1240\_84 a1240a\_176 a1280\_160  
a1280\_172 a1280\_176 a1280a\_84 a14100\_208 a14100\_256 a14100\_257 a14100\_313  
a1415a\_100 a1415a\_84 a1425\_133 a1425\_160 a1425\_84 a1425a\_100 a1425a\_100v  
a1425a\_132 a1440a\_100 a1440a\_160 a1440a\_175 a1440a\_176 a1440a\_84 a1460\_207  
a1460\_208 a1460a\_160 a1460a\_176 a1460a\_196 a1460a\_225 a32140dx\_160  
a32140dx\_176 a32140dx\_208 a32200dx\_pq208 a32200dx\_rq208 a32200dx\_rq240  
a3265dx\_160 a3265dx\_176 a3265dx\_84 a40mx02\_100 a40mx02\_68 a40mx02\_80  
a42mx09\_100 a42mx09\_160 a42mx09\_176 a42mx09\_84 a42mx16\_100 a42mx16\_160  
a42mx16\_176 a42mx16\_208 a42mx16\_84 a42mx24\_160 a42mx24\_176 a42mx24\_208  
a42mx24\_84 a42mx36\_208 a42mx36\_240 a42mx36\_272 a54sx08\_100 a54sx08\_144  
a54sx08\_176 a54sx08\_208 a54sx16\_100 a54sx16\_176 a54sx16\_208 a54sx16\_256  
a54sx16p\_144 a54sx32\_144 a54sx32\_176 a54sx32\_208 a54sx32\_313 att1c03\_100  
att1c03\_132 att1c03\_208 att1c03\_225 att1c03\_84 att1c05\_100 att1c05\_132  
att1c05\_208 att1c05\_225 att1c05\_240 att1c05\_84 att1c07\_208 att1c07\_240  
att1c07\_280 att1c07\_304 att1c09\_208 att1c09\_240 att1c09\_304 att2c04\_100  
att2c04\_144 att2c04\_160 att2c04\_208 att2c04\_84 att2c06\_100 att2c06\_144  
att2c06\_160 att2c06\_208 att2c06\_240 att2c06\_84 att2c08\_160 att2c08\_208  
att2c08\_240 att2c08\_256 att2c08\_304 att2c08\_84 att2c10\_160 att2c10\_208  
att2c10\_208 att2c10\_240 att2c10\_256 att2c10\_304 att2c10\_84 att2c12\_208  
att2c12\_240 att2c12\_256 att2c12\_304 att2c12\_365 att2c15\_208 att2c15\_240  
att2c15\_304 att2c15\_365 att2c26\_208 att2c26\_240 att2c26\_304 att2c26\_428  
att2c40\_208 att2c40\_240 att2c40\_304 att2c40\_428 att3020\_100 att3020\_68 att3020\_84  
att3030\_100\_j att3030\_100\_t att3030\_44 att3030\_68 att3030\_84 att3042\_100\_j  
att3042\_100\_t att3042\_132 att3042\_144 att3042\_84 att3064\_100 att3064\_132  
att3064\_144 att3064\_160 att3064\_84 att3090\_160 att3090\_175 att3090\_84 atv2500b  
cy7c361 cy7c371 cy7c372 cy7c373 cy7c374 cy7c375 ep1k100\_208 ep1k100\_256  
ep1k100\_484 ep1k10\_144 ep1k10\_208 ep1k30\_144 ep1k30\_208 ep1k30\_256  
ep1k50\_144 ep1k50\_208 ep1k50\_256 ep1k50\_484 ep20k1000e\_33 ep20k1000e\_652  
ep20k1000e\_672 ep20k100\_144 ep20k100\_208 ep20k100\_240 ep20k100\_324  
ep20k100\_356 ep20k100e\_144 ep20k100e\_208 ep20k100e\_240 ep20k100e\_324  
ep20k100e\_356 ep20k100e\_fc144 ep20k1500e\_33 ep20k1500e\_652 ep20k160e\_144  
ep20k160e\_208 ep20k160e\_240 ep20k160e\_356 ep20k160e\_484 ep20k200\_208  
ep20k200\_240 ep20k200\_356 ep20k200\_484 ep20k200e\_208 ep20k200e\_240  
ep20k200e\_356 ep20k200e\_484 ep20k200e\_652 ep20k200e\_672 ep20k300e\_208  
ep20k300e\_240 ep20k300e\_652 ep20k300e\_672 ep20k30e\_144 ep20k30e\_208  
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ep20k400e\_652 ep20k400e\_672 ep20k600e\_33 ep20k600e\_652 ep20k600e\_672  
ep20k60e\_144 ep20k60e\_208 ep20k60e\_240 ep20k60e\_324 ep20k60e\_356  
ep20k60e\_fc144 epf10k100\_240 epf10k100\_503 epf10k100a\_356 epf10k100a\_484  
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epf10k100e\_256 epf10k100e\_356 epf10k100e\_484 epf10k10\_144 epf10k10\_208  
epf10k10\_84 epf10k10a\_100 epf10k10a\_256 epf10k130\_599 epf10k130e\_240  
epf10k130e\_484 epf10k130e\_600 epf10k130e\_672 epf10k130v\_600 epf10k200e\_599  
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epf10k50e\_256 epf10k50e\_484 epf10k50s\_144 epf10k50s\_208 epf10k50s\_356  
epf10k50s\_484 epf10k70\_240 epf10k70\_503 epf6010a\_144 epf6016\_100 epf6016\_144  
epf6016\_208 epf6016\_240 epf6016\_256 epf6016a\_144 epf6016a\_208 epf6024a\_144  
epf6024a\_208 epf6024a\_240 epf6024a\_256 epf6024a\_f256 epf81188\_208  
epf81188\_232 epf81188\_240 epf81500\_280 epf81500\_304 epf81500a\_240  
epf8282\_100 epf8282\_84 epf8452\_160 epf8452\_84 epf8452a\_100 epf8636\_160  
epf8636\_192 epf8636\_208 epf8636\_84 epf8820\_144 epf8820\_160 epf8820\_192  
epf8820\_208 epf8820\_225 epm3032a\_44 epm3032a\_t44 epm3064a\_100 epm3064a\_44  
epm3256a\_144 epm3256a\_208 epm5016 epm5032 epm5064 epm5128 epm5130  
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isplsi5384v\_208 isplsi5384v\_272 isplsi5384v\_388 isplsi5512v\_388 mach110 mach111  
mach111sp mach120 mach130 mach131 mach210 mach211 mach211sp mach215  
mach220 mach221 mach221sp mach230 mach231 mach231sp mach355 mach435  
mach436 mach445 mach446 mach446jedec mach465 mach466 mach4\_128\_64  
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or3t30\_352 or3t55\_208 or3t55\_240 or3t55\_256 or3t55\_352 or3t80\_208 or3t80\_240  
or3t80\_352 or3t80\_432 or3t80\_600 p12x16\_100 p12x16\_68 p12x16\_84 p16x24b\_100  
p16x24b\_144 p16x24b\_84 p24x32b\_144 p24x32b\_208 p24x32b\_223 p8x12\_100  
p8x12\_44 p8x12\_68 plsi1016 plsi1016e\_44 plsi1024 plsi1032 plsi1032e\_84 plsi1048  
plsi1048c\_128 plsi2032\_44 plsi2064\_100 plsi2064\_84 plsi2096\_128 plsi2128\_160  
plsi3160\_208 plsi3192\_240 plsi3256\_160 plsi3256\_167 plsi3256a\_160 plsi3256e\_304  
plsi3320\_208 ql12x16\_100 ql12x16\_68 ql12x16\_84 ql8x12\_100 ql8x12\_44 ql8x12\_68  
xc2018 xc2018\_68 xc2064 xc2064\_48 xc2s100\_144 xc2s100\_208 xc2s100\_256  
xc2s100\_456 xc2s150\_208 xc2s150\_256 xc2s150\_456 xc2s15\_100 xc2s15\_144  
xc2s15\_144tq xc2s200\_208 xc2s200\_256 xc2s200\_456 xc2s30\_100 xc2s30\_144  
xc2s30\_144tq xc2s30\_208 xc2s50\_144 xc2s50\_208 xc2s50\_256 xc2v10000\_957  
xc2v1000\_256 xc2v1000\_456 xc2v1000\_575 xc2v1000\_896 xc2v1500\_575  
xc2v2000\_575 xc2v2000\_728 xc2v2000\_957 xc2v250\_256 xc2v250\_456  
xc2v3000\_676 xc2v3000\_957 xc2v4000\_957 xc2v500\_256 xc2v500\_456  
xc2v6000\_1152 xc2v6000\_957 xc2v8000\_957 xc3020 xc3020\_68 xc3030 xc3030\_44  
xc3030\_68 xc3030\_84 xc3042 xc3042\_100 xc3042\_144 xc3042\_84 xc3064  
xc3064\_132 xc3064\_144 xc3064\_84 xc3090 xc3090\_160 xc3090\_164 xc3090\_176  
xc3090\_208 xc3090\_84 xc3195\_160 xc3195\_175 xc3195\_208 xc3195\_223 xc3195\_84  
xc4002a\_100 xc4002a\_120 xc4002a\_84 xc4002xl\_100 xc4003\_100 xc4003\_120  
xc4003\_84 xc4003e\_100 xc4003e\_120 xc4003e\_84 xc4003h\_191 xc4003h\_208

xc4004a\_120 xc4004a\_144 xc4004a\_160 xc4004a\_84 xc4005\_144 xc4005\_156  
xc4005\_160 xc4005\_164 xc4005\_208 xc4005\_84 xc4005e\_100 xc4005e\_144  
xc4005e\_156 xc4005e\_160 xc4005e\_208 xc4005e\_84 xc4005h\_223 xc4005h\_240  
xc4005xl\_100 xc4005xl\_144 xc4005xl\_160 xc4005xl\_208 xc4005xl\_84 xc4006\_156  
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xc4010xl\_208 xc4010xl\_256 xc4010xl\_84 xc4013\_160 xc4013\_208 xc4013\_223  
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xc4044xl\_352 xc4044xl\_411 xc4044xl\_432 xc4044xla\_160 xc4044xla\_208  
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xc95288xl\_bg256 xc9536\_44 xc9536xl\_44 xc9572\_100 xc9572\_84 xc9572xl\_100  
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xcv1000\_560 xcv1000\_680 xcv1000e\_1156 xcv1000e\_240 xcv1000e\_560  
xcv1000e\_680 xcv1000e\_728 xcv1000e\_860 xcv1000e\_900 xcv100\_228 xcv100\_240  
xcv100\_256 xcv100\_cs144 xcv100\_fg256 xcv100\_tq144 xcv100e\_144 xcv100e\_240  
xcv100e\_256 xcv100e\_352 xcv150\_240 xcv150\_352 xcv150\_456 xcv150\_bg256  
xcv150\_fg256 xcv1600e\_1156 xcv1600e\_560 xcv1600e\_680 xcv1600e\_860  
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xcv50\_cs144 xcv50\_tq144 xcv50e\_144 xcv50e\_240 xcv50e\_256 xcv600\_228  
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xcv800\_432 xcv800\_560 xcv800\_676 xcv800\_680 xcv812e\_560 xcv812e\_900

# From Previous Release Notes

## SystemC/SWIFT Support Changes

SystemC/SWIFT now uses SystemC release 2.0.1. It was developed on Red Hat Linux 6.2 with gcc 2.95.3 and on Solaris 2.6 also with gcc 2.95.3. Supported platforms now only include Red Hat Linux 6.2 and 7.2 (with gcc 2.95.3). This is because Solaris 2.6 is no longer supported.

For information on how to use SmartModels and FlexModels with SystemC, see the [SmartModel Library Application Notes Manual](#).

## Migration of Cyclone and VSS Users to Scirocco

On September 24, 2001 Synopsys informed Cyclone and VSS customers of the Synopsys plan to migrate to Scirocco and obsolete Cyclone and VSS.

## New Tool, `cnvt2mif`

A new tool, `cnvt2mif`, replaces `mi_trans` for converting memory data files to the memory image file (MIF) format. Using `cnvt2mif`, you can optionally specify the number, name, and bit width of output files and perform endian conversion. In addition, you can select data from within the input file by specifying an address range for the conversion. You can also specify a base address for indexed addressing, and control the verbosity and extent of message display. `cnvt2mif` reads hexadecimal digits in either upper or lower case. You should use `cnvt2mif` for new designs, but `mi_trans` is still supported for backward compatibility. For more details see the [SmartModel Library User's Manual](#).

## Supporting 32-Bit Libraries on 64-Bit Platforms

If you want to run 32-bit Synopsys models or tools on a 64-bit HP-UX or Solaris platform, set the `LMC_USE_32BIT` environment variable to any value before invoking the tool, as shown in the following example:

```
% setenv LMC_USE_32BIT 1
```

The `LMC_USE_32BIT` environmental variable is a “set/no-set” variable. That is, you can set it to any value (even zero) to turn on 32-bit support on a 64-bit platform. If you do not set it at all, the default condition is 32-bit models on 32-bit platforms, or 64-bit models on 64-bit platforms. You only set this environmental variable (to any value) when you are on a 64-bit platform using 32-bit models and simulators.

# FlexModel Issues and Workarounds

Following are known issues with the FlexModel software, along with suggested workarounds:

- When using multiple instances of a FlexModel within one or more top-level Verilog testbenches (VCS, Verilog-XL,...) you may see the message:

```
Error: undefined symbol "flex_<cmd name>" (<testbench> line <number>)
```

To work around this error:

- a. Add the line

```
`undef FLEXMODEL_CMDS_INC
```

before the line that reads

```
`include model_pkg.inc
```

- b. On the simulator invocation line, add the multi-instance specification to your invocation.

```
+define+flex_multi_inst
```

- The *model\_set\_pin* commands do not work in timing mode. The observed behavior is that certain pins do not set. We recommended that you do not use this command when timing mode is turned on.
- Do not use multiple HDL command streams to control a single FlexModel instance. This may cause unpredictable behavior.
- The following note applies to QuickSim customers who use symbol files shipped with Synopsys FlexModels. FlexModel pins are mapped to a dummy DIP package that the real device may not come in. If you want to use it for connectivity to drive a board netlist, you should create your own mapping to a real package configuration of the device you are using. In addition, all of the voltage and current information in the symbol file is set to default. No attempt was made to create an accurate symbol file; it is only a place holder.
- If you get an error message similar to the following example, you need to recompile your C testbench. (This message appears as an exception in the transcript window.)

```
C interface versions of flexmodel_pkg(1) & fastm_cmdcore(2) do not match
```

This error occurs when your testbench has been compiled with an earlier version of *flexmodel\_pkg* and you have updated your LMC\_HOME tree with the latest *flexmodel\_pkg* and Command Core. For information on how to recompile a C testbench, see the [FlexModel User's Manual](#).

## Getting Help

If you have a question about using Synopsys products, please consult product documentation that is installed on your network or located at the root level of your Synopsys product CD-ROM (if available). You can also access documentation for DesignWare products on the Web:

- Product documentation for many DesignWare products:

<http://www.synopsys.com/products/designware/docs>

- Datasheets for individual DesignWare IP components:

<http://www.synopsys.com/products/designware/ipdir>

You can also contact the Synopsys Support Center in the following ways:

- Open a call to your local support center using this Web page:

<http://www.synopsys.com/support/support.html>

- Send an e-mail message to [support\\_center@synopsys.com](mailto:support_center@synopsys.com).

- Telephone your local support center:

- United States:

Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific Time, Mon—Fri.

- Canada:

Call 1-650-584-4200 from 7 AM to 5:30 PM Pacific Time, Mon—Fri.

- All other countries:

Find other local support center telephone numbers at the following URL:

[http://www.synopsys.com/support/support\\_ctr](http://www.synopsys.com/support/support_ctr)

## Additional Information

For additional Synopsys documentation, refer to the following page:

<http://www.synopsys.com/products/designware/docs>

For up-to-date information about the latest implementation IP and verification models, visit the IP Directory:

<http://www.synopsys.com/products/designware/ipdir>

## The Synopsys Web Site

General information about Synopsys and its products is available at this URL:

<http://www.synopsys.com>

## Comments?

To report errors or make suggestions, please send e-mail to:

[doc@synopsys.com](mailto:doc@synopsys.com)

To report an error that occurs on a specific page, select the entire page (including headers and footers), and copy to the buffer. Then paste the buffer to the body of your e-mail message. This will provide us with information to identify the source of the problem.